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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/507,283	09/10/2004	Bernd Arenz	521.1035	2853

23280 7590 01/12/2006

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NEW YORK, NY 10018

EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/507,283	ARENZ ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Durviage, EP 0440764 B1. With respect to Claims 10 and 20, Durviage [EP 0440764B1] teaches a circuit breaker [Fig. 1] comprising: a main contactor [Fig. 1, contactor 114]; a current detector [Fig. 1, analog input circuit 108 and ground fault sensor 110] configured to provide test signals of a current to be monitored via the main contactor; a microprocessor-controlled tripping device [Fig. 1, page 3, lines 26-27] including a microprocessor [Fig. 1 microcomputer 120] and a watchdog circuit configured to monitor the microprocessor [Fig. 1, watchdog and reset 124], the tripping device being configured to receive energy from the current detector [Fig. 1, solenoid 112, page 3 lines 29-31 and page 9, lines 5-6] to process the test signals and to activate a tripping coil [Fig. 4, solenoid trip coil 112] so as to automatically open the main contactor when a settable limit value [page 3 lines 44-46; page 4 lines 14-17] is exceeded;

a bypass circuit [~~formed by the watchdog circuit and the tripping system~~] configured to receive energy from the current detector [page 9, lines 5-6 and page 12, lines 30-32] and including a high pass filter connected downstream from

the watchdog circuit [Fig. 4, capacitor 584 with transistor 568 filters the voltage ripple, page 9 lines 22-24], a first semiconductor switch connected downstream from the high pass filter [Fig. 4, IGFET 583, page 9 lines 24-26], a charging capacitor dischargeable via the first semiconductor switch [Fig. 4, capacitor 574 page 9 lines 22-28], and a voltage comparator [Fig. 8, comparator 726] having a first input [negative of comparator 726], a second input [positive of comparator 726] and an output side, the voltage comparator being connected via the first input to the current detector [Fig. 8, current signal from resistor 729] and on the output side to the charging capacitor [Fig. 4, charging capacitor 574 page 9 lines 24-26];

a monitoring circuit configured to apply a first reference voltage to the second input of the comparator when a supply voltage is below a pre-defined threshold level and to apply a second reference voltage to the second input of the comparator when the supply voltage is above the pre-defined threshold level, the first reference voltage being associated with a first current limit value and the second reference voltage being associated with a second current limit value that is smaller than the first current limit value, with the first and second reference voltage being formed by changes in the power supply to the zener diode that are caused by the opening and closing of the contactor; and

an actuation circuit [Fig. 4, 587 and 589] connected on an output side thereof to the tripping coil and configured to be actuated via a first OR-input by the tripping device and via a second OR-input by the charging capacitor as a

function of a state of charge of the charging capacitor [Fig. 4 either microcomputer 120 or watchdog and reset 124 can actuate solenoid 112- page 9 lines 22-28].

With respect to Claims 11and 21, Durviage teaches that the first current limit value corresponds to a maximum settable limit value for a tripping current of the circuit breaker.

With respect to Claims 12 and 20, Durviage teaches that the monitoring circuit is configured to apply the first reference voltage to the second input of the voltage comparator before a lapsing of a threshold time calculated from a time when the circuit breaker is switched on and to apply the second reference voltage to the second input of the comparator after the lapsing of the threshold time.

With respect to Claims 13 and 22, Durviage teaches that the bypass circuit includes a first pulse shaper stage [Fig. 8, diode 732, in addition with capacitor 718 and resistor 730, functions as the pulse shaper to produce logic signals for switch 720 - page 12, lines 33-36] connected between the high pass filter and the first semiconductor switch.

Claims 14 and 23, Durviage teaches that the bypass circuit includes a second pulse shaper stage connected between the charging capacitor and the actuation circuit [Fig. 4, the diode shown between charging capacitor 574 and solenoid trip coil 112 functions to shape the output of capacitor 574 before it enters the trip coil 112].

With respect to Claims 15 and 24, Durviage teaches that the bypass circuit includes an electronic change-over switch [Fig. 8, switch 720 functions as a changeover switch] capable of being switched over by the monitoring circuit [switch 720 is switched by pulses from microcomputer 120], the monitoring circuit being configured to feed the first [Fig. 8, Vref from resistor 729] and the second reference voltages [the voltage across charged/discharged capacitor 735] to the comparator [Fig. 8, comparator 726] via the electronic change-over switch .

With respect to Claims 16 and 25, Durviage teaches that the watchdog circuit is configured to provide watchdog pulses, and further comprising a pulse suppression device [Fig. 8, power up reset 710 with switch 720; page 12, lines 14-20] controllable by the monitoring circuit and configured to suppress the watchdog pulses when the supply voltage is below the pre-defined threshold value [page 12, par. D Reset Circuitry].

With respect to Claims 17 and 26, Durviage teaches that the pulse suppression device includes a second semiconductor switch [Fig. 8, switch 720 supplies a signal through diode 753] connected to an output side of the high pass filter [capacitor 584 and transistor 568 form a high pass filter].

With respect to Claims 18 and 27, Durviage teaches that the watchdog circuit is configured to provide watchdog pulses, and further comprises a pulse suppression device configured to suppress the watchdog pulses [Fig. 8, power up reset 710 with switch 720; page 12, lines 14-20].

With respect to Claims 19 and 28, Durviage discloses that the pulse suppression device includes a second semiconductor switch connected to an output side of the high pass filter [capacitor 584 and transistor 568 form a high pass filter].

Conclusion

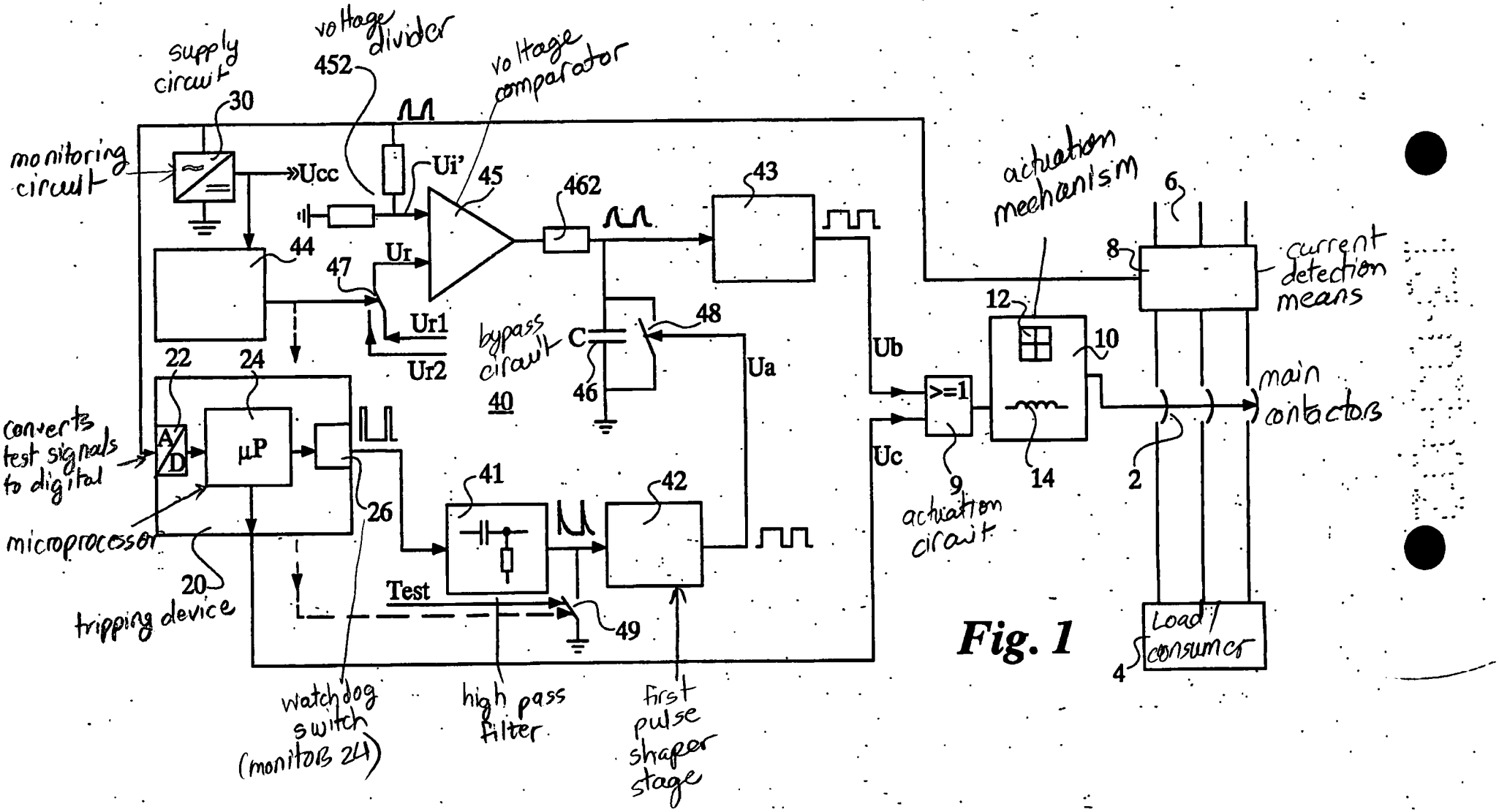
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jensen [US Patent No. 5,214,560] is cited for the disclosure of a similar microprocessor watchdog circuit that is monitored via pulses, for electronic trip units.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

PHUONG T. VU
PRIMARY EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
01/03/2006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A/D
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converts test signals to digital
microprocessor
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tripping device
26
41
42
Test
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watchdog switch (monitors 24)
high pass filter
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14
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6
8
current detection means
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main contactors
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4

Fig. 1

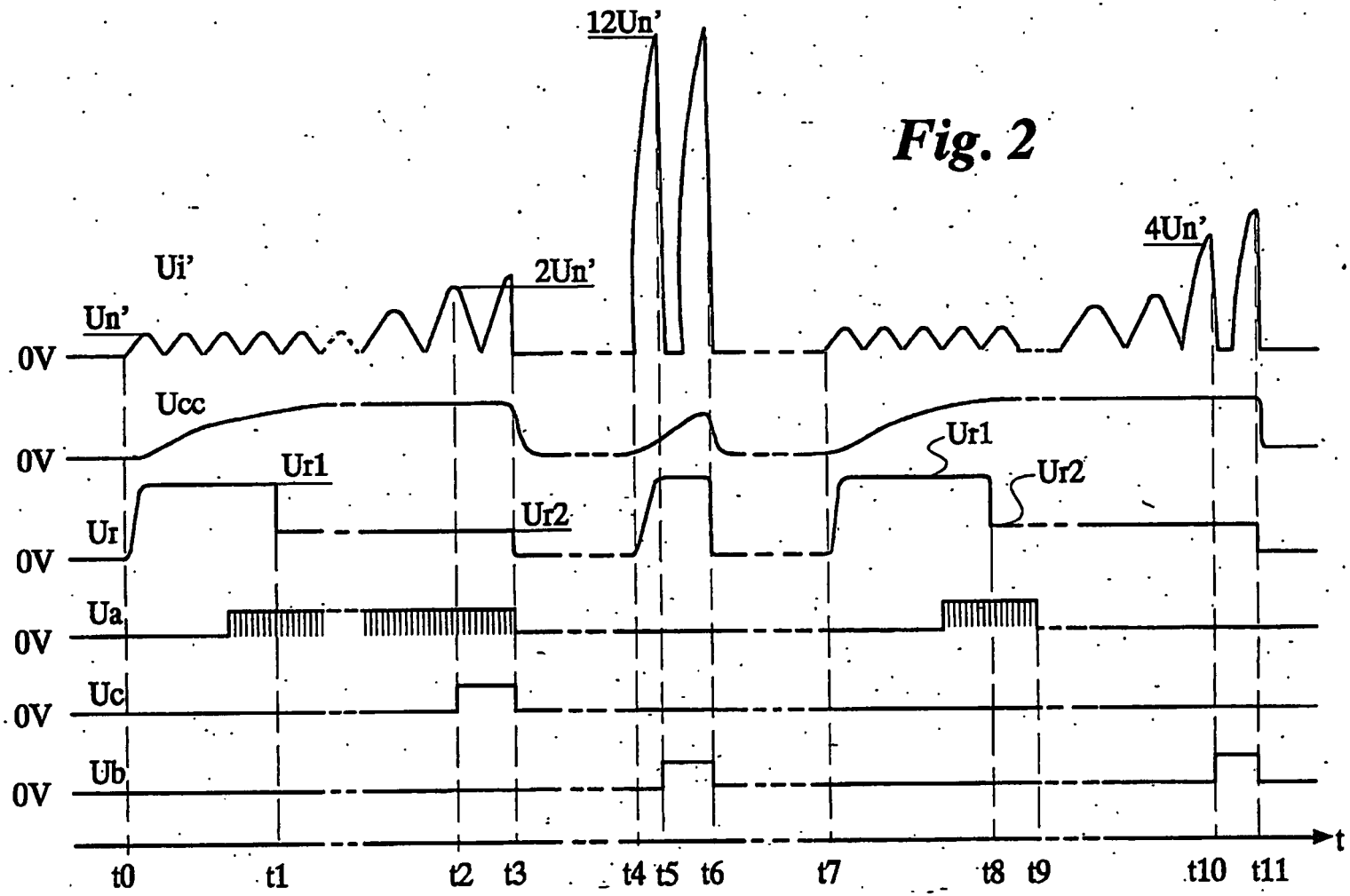
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Fig. 2